High-Frequency Si-MOSFET's

C. TSIRONIS AND U. NIGGEBRÜGGE

Abstract—**Silicon (Si-) MOSFET's with 0.8-μm channel, made by conventional technology and optimized for microwave applications, have noise figures of 3.7 dB at 4 GHz and maximum frequencies of oscillation of 10 to 12 GHz. The noise and radio-frequency (RF) small signal performance are only slightly affected by double ion implantation of the channel region, used to shift the threshold voltage from −2 V to +0.2 V. Excess noise is generated in the implanted MOSFET's for lower V_{DS} values than in unimplanted ones. The variation of the noise parameters with drain current is lower in implanted devices. The RF equivalent circuit analysis indicates negligible parasitic lead resistances, but high feedback capacitance. A comparison with GaAs MESFET's of the buried channel type showed the Si-MOSFET's to have lower third-order harmonic distortion when driven by a 1-GHz signal source.**

I. Introduction

Si-MOSFET'S are primarily used in digital circuits and at frequencies below 1 GHz. Parasitics caused by the nonsatisfactory isolation of the substrate material and the lower mobility of silicon in comparison with GaAs limit the high-frequency performance of these devices and many precautions must be taken concerning the structure and layout in order to realize gigahertz MOSFET's. By optimization of the technology and device geometry *n*-channel enhancement Si-MOSFET's have been realized with usable characteristics of up to 6 GHz [1]. It has been shown that the use of ion implantation to overcome two-dimensional effects like negative threshold voltages and low punchthrough enables the realization of normally off MOSFET's and has no significant effect on the RF and noise device behavior. Only the biaspoint dependence of the noise parameters is not negligibly affected by ion implantation. A numerical model analysis of a modified structure, based on the determined equivalent circuit, shows a higher stability frequency range and maximum frequencies of oscillation of 13 to 14 GHz to be possible for these devices by avoiding gate overlap. Further advantages of the Si-MOSFET's (especially in comparison with GaAs devices) are the high uniformity in dc and radio-frequency (RF) behavior and the high reliability resulting from the mostly well-developed technology. The absence of low-frequency trapping effects causes a negligible drifting in time of the device characteristics.

II. Device Technology, DC Characteristics

The n-channel MOSFET's have been fabricated using mostly conventional technology. The drain and source inlaid regions were made by phosphorous diffusion, the gate and masking oxides were made by thermal oxidation, and optical projection printing was used.

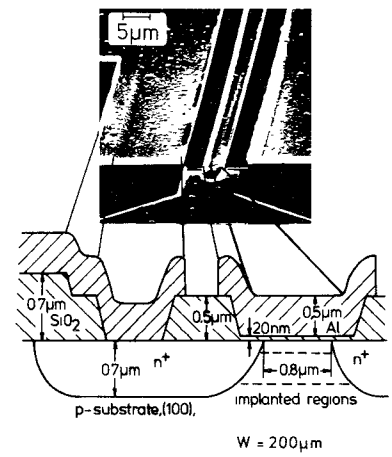

Fig. 1. Cross section of MOSFET structure and SEM picture of the central region.

Fig. 1 gives a schematic cross section of the MOSFET-inner region and a SEM picture of the active device part. The following technology parameters were chosen to optimize the MOSFET high-frequency behavior: Short channel length of 0.8 μm for very small transit time in connection to the high mobility of the carriers in n-type inversion layers. The channel length was estimated from mask dimensions and lateral diffusion depth. The equivalent circuit analysis (Section III) predicts a transit time of the order of 6 ps (Fig. 8). The linear increase of drain current with gate voltage in the characteristics of Fig. 2 predicts the conducting carriers to have reached their saturation drift velocity $v_{sat} \approx 10^7$ cm·s^{-1} for $V_{DS} \approx 2$–3 V (depending on V_{GS}). So the effective channel length can be calculated to

$$L_{eff} = v_{sat} \cdot \tau \approx 0.6\ \mu\text{m}. \tag{1}$$

A thin gate oxide was used (≈200 Å) to achieve high transconductance. The input capacitance, calculated from

$$C_{in} \approx \frac{2}{3} \cdot \frac{z \cdot L \cdot \epsilon}{t_{ox}} \approx 0.18\ \text{pF} \tag{2}$$

with $z = 200$-μm device width; $L = 0.8$-μm channel length; $\epsilon = \epsilon_0 \cdot \epsilon_r = 33.6 \cdot 10^{-14}$F/cm; and $t_{ox} = 200$-Å oxide thickness. The value $C_{gs} = 0.3$ pF, found by the small signal equivalent circuit analysis (Fig. 8), is in good agreement with the theoretical predictions, since in C_{gs} also capacitive parts due to overlapping of the gate and source electrode and bonding path parasitics are included.

A low doped substrate of $N_A \approx 1.2 \cdot 10^{15}$ cm^{-3}, small gate-drain overlap of 0.4 μm, and thick field oxide of 0.7

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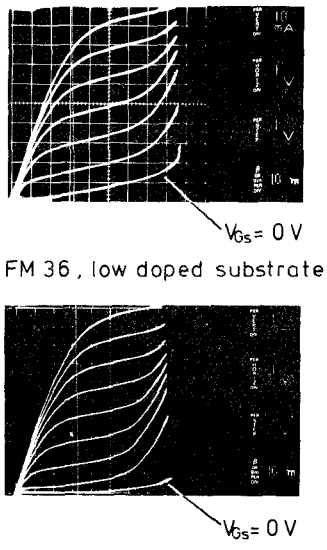

Fig. 2. DC-output characteristics of Si-MOSFET's. Devices FM 38, FM 39, and FM 40 are double implanted.

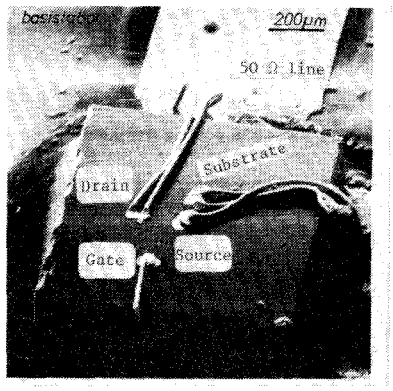

Fig. 3. SEM picture of the bonded chip on Al_2O_3 substrate. Chip dimensions are $0.9\times0.75\times0.4$ mm^3. The MOSFET ohmic contacts are 200×10 μm^2 and the device width is 200 μm.

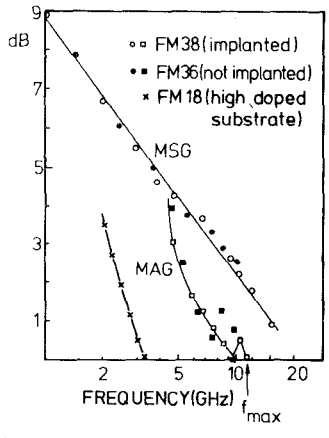

Fig. 4. Measured MSG and MAG values of Si-MOSFET's with a channel length of 0.8 μm.

μm, sputtered after diffusion, were used to reduce the parasitic capacitances. The bonding path capacitances were also kept as small as possible. To achieve negligible gate lead resistances, important at very high frequencies, aluminium gate technology was preferred to a self-aligning polysilicon one.

The use of low doped substrates for structures with drain-source distances below 2 μm causes a shift of threshold to negative values and leakage currents resulting from punchthrough. To minimize these effects, the dopant concentration was raised only in the channel region via boron ion implantation, after etching the gate ditch and depositing the gate oxide.

For comparison purposes nonimplanted devices were also fabricated (FM 36). The implantation energy was 30 keV and the dose 10^{12} cm^{-2}, resulting in a threshold shift from -2 V for unimplanted devices to $+0.2$ V for implanted ones (FM 37). A series of MOSFET's received an additional deeper boron implantation with an energy of 110 keV and a dose of $2\text{–}8\cdot10^{11}$ cm^{-2} to increase the punchthrough voltage (FM 38, 39, and 40). Unimplanted devices already showed punchthrough behavior above zero drain-source voltage. By implantation the punchthrough point could be raised up to 5 V at $V_{GS}=V_{sub}=0$ V.

Fig. 2 gives a typical dc output characteristic of implanted and unimplanted MOSFET's indicating, besides the threshold voltage shift, the high linearity and the excess current region of the implanted devices to occur earlier as in the unimplanted ones (see also Section IV).

III. AC Behavior

A. RF Characteristics

For RF characterization the MOSFET chips were mounted on 0.65-mm thick alumina substrate and bonded to 50-Ω gold microstrip lines as Fig. 3 shows. The substrate was connected to source by parallel bonding between the substrate bonding path and earth, passed through a hole from the backside of the substrate by conducting epoxy. Scattering parameter measurements were carried out in the frequency range of 1–14 GHz [2]. Fig. 4 shows maximum available gain (MAG) and maximum stable gain (MSG) values for three different MOSFET types. Ion implantation of the channel region affects the MAG and the unilateral gain UG (after Mason) behavior of the MOSFET's only slightly. On the other hand, a high doped substrate, used for higher punchthrough V_{DS} values, gives f_{max} of 3.3 GHz.

The local peak in the MAG (f) characteristic of the MOSFET's at 8–10 GHz has its origin in internal feedback due to the high gate-drain capacitance, as will be shown later. As computer simulation showed, the gain peak diminishes for $C_{gd}<0.1$ pF. Fig. 5 confirms the good simulation of the RF behavior of the MOSFET's by the equivalent circuit of Fig. 8, by means of comparison of measured and calculated MAG, UG, k, and $|S_{21}|^2$ values. Here k is the stability factor after Rollett.

On the basis of the present model (Fig. 7) we calculated the improvement in gain performance for an implanted MOSFET FM 40 achievable by avoiding overlap of the gate to the drain and source electrodes. A MOSFET structure with a recessed gate [3] will be possible using e-beam lithography. Assuming the new structure (upper side of Fig. 6(a), (b)) to have lower gate to drain and gate

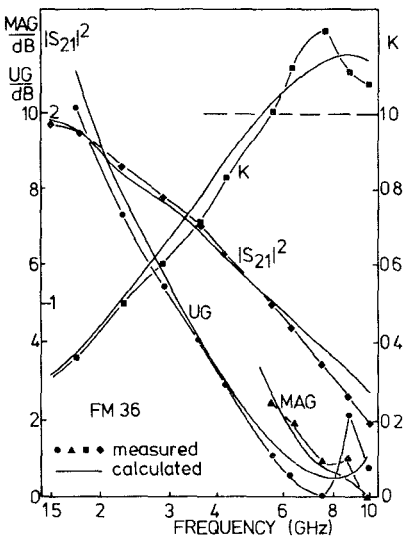

Fig. 5. Measured and simulated gain and stability parameters of an unimplanted Si-MOSFET, FM 36, $V_{DS}=4$ V, $V_{GS}=4$ V, and $I_D=48$ mA.

to source capacitances with

$$C'_{gd}=\alpha\cdot C_{gd}, \qquad C'_{gs}=\beta\cdot C_{gs} \tag{3}$$

$\beta\approx\frac{2}{3}$, $\alpha\approx\frac{1}{3}-\frac{1}{4}$, we found the gain and stability behavior given in Fig. 6 by dotted lines. As can be seen, the maximum frequency of oscillation can be increased by 3 GHz and the MAG reaches a 2.5-dB higher value at 6 GHz. Devices with the present structure and f_{max} of 10 to 11 GHz should reach, after shortening, an f_{max} of 13 to 14 GHz.

Assuming the transconductance to be unaffected by the new structure, the transit frequency of the intrinsic device

$$f_\tau=\frac{g_m}{2\pi\cdot C_{gs}} \tag{4}$$

would be increased from 6.4 GHz to 9.5 GHz. The increase of f_{max} comes from the reduction of C_{gs}, whereas the reduction of C_{gd} spreads the useful stable frequency range of operation of the MOSFET's (Fig. 6).

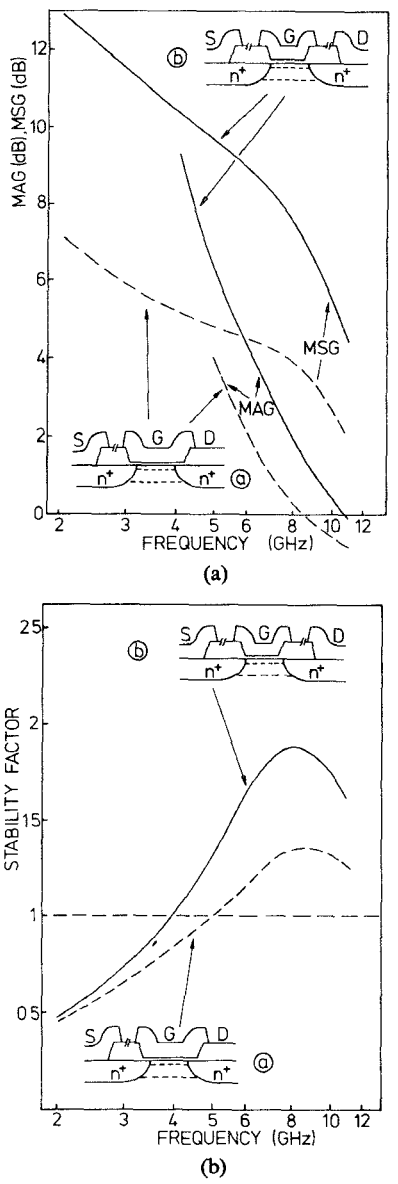

Fig. 6. (a) Calculated gain and stability behavior of present (a:_____) and (b) planned MOSFET structures with nonoverlapping of the gate (b:_____). Device data of FM 40.

B. Equivalent Circuit

To determine the principal structure of the MOSFET-equivalent circuit, lumped elements were inserted into the schematic cross section of the device as given in Fig. 7. The series resonant circuit between drain and source through the substrate contact serves for better simulation of the output reflection coefficient S_{22} (Figs. 3 and 9). The capacitances C_{gd} and C_{gs} include parts due to overlap of the electrodes.

The element values of the small signal equivalent circuit of the Si-MOSFET's were determined from measured scattering parameters at 10 frequencies between 1 and 10 GHz by computer minimization of an error function (EF) defined as

$$EF=\left\{\sum_{f_1}^{f_{10}}\sum_{i,j}|S_{ij}(f_k)_m-S_{ij}(f_k)_c|^2\Big/\sum_{f_1}^{f_{10}}\sum_{i,j}|S_{ij}(f_k)_m|^2\right\}^{1/2} \tag{5}$$

where f_k is the kth frequency, and $S_{ij}(f_k)_m$ and $S_{ij}(f_k)_c$ the measured and calculated values of the corresponding s-parameters, respectively. The lowest values of the simulation EF were 5 to 9 percent. In Fig. 8 the computed values of the elements of the equivalent circuit of Fig. 7 are given for a double implanted MOSFET FM 38 as average values of several optimization runs for this type of device. The achieved agreement between measured and calculated s-parameters is given in Fig. 9. The exact simulation of S_{12} and S_{22} should be noticed, the first one corroborating the found magnitude of C_{gd} and the last one being possible only by inserting the $C_{ds}-R_{ds}-L_{ds}$ series path at the device output. The EF has in this case a value of 5.1 percent.

The simulation of gain and stability parameters for an unimplanted MOSFET (FM 36) is given in Fig. 5. The agreement is good though the EF has a value of 9.5

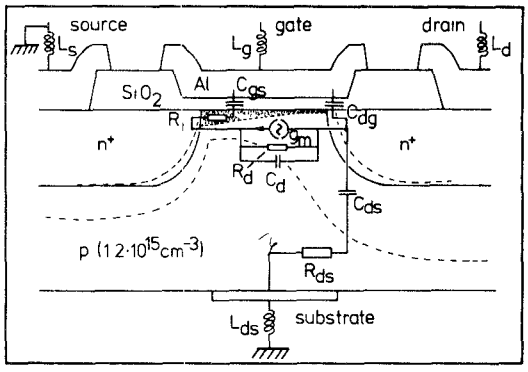

Fig. 7. Schematic cross section of the MOSFET's with incorporated lumped elements to determine the equivalent circuit.

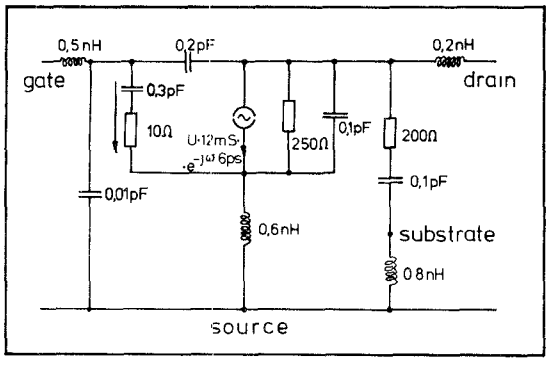

Fig. 8. Equivalent circuit of Si-MOSFET FM 38 (double implanted) with element values estimated from several optimization runs for this type of device.

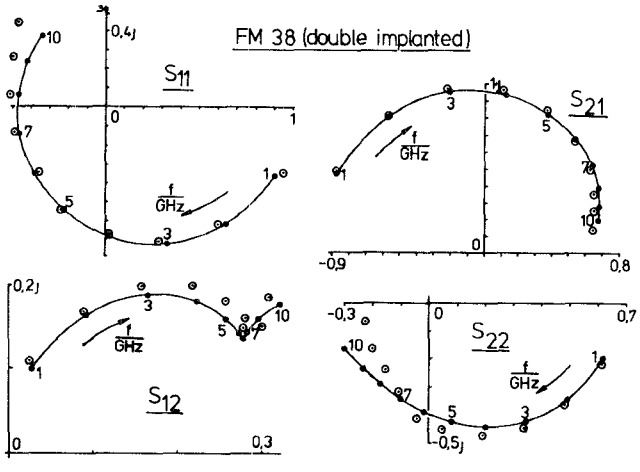

Fig. 9. Comparison of measured and calculated values of scattering parameters for MOSFET FM 38; ●: calculated, ⊙: measured points.

percent. The most important results of the small signal equivalent circuit analysis are the following.

a) The parasitic lead resistances between the inner MOSFET and the gate, source, and drain contacts can be neglected. Although for these parasitic resistances finite starting values of 2 to 6 Ω were chosen for the optimization procedure, the result was in every case $R_S \to 0$, $R_D \to 0$, $R_G \to 0$. In the calculations of Fig. 6 a drain lead resistance of 2 Ω was chosen when the gate and drain do not overlap.

b) The gate-to-drain capacitance is between 0.2 and 0.3 pF for all calculated equivalent circuits. This is nearly 5 to

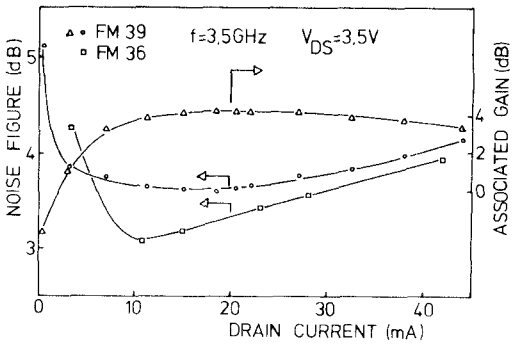

Fig. 10. Dependence of noise figure and associated gain on drain current.

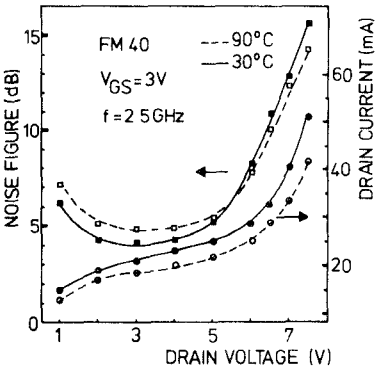

Fig. 11. Dependence of noise figure and drain current on drain voltage. 90°C and 30°C are the alumina substrate temperatures. The chip temperature should be slightly higher, depending on I_D.

10 times larger than the corresponding value of a Si-MESFET [4] and limits the useful stable frequency range of the MOSFET's (Fig. 6). The magnitude of $S_{21}(f)$ was constant for frequencies between 0 and 300 MHz, meaning that there are no problems with interface states as reported in [5] for GaAs MOSFET's.

IV. Noise, Large Signal, and Pulse Behavior

A. Noise Parameters of the Si-MOSFET's

The noise behavior of the Si-MOSFET's was experimentally investigated in the frequency range between 2 and 6 GHz, since at higher frequencies the gain available from the devices is poor.

Measuring the noise figure at 12 different source admittances Y_s with a measuring setup as given in [6] we could determine all 4 noise parameters of the MOSFET-two-port as defined by (6):

$$F = F_o + \frac{R_n}{\mathrm{Re}(Y_s)} \cdot |Y_s - Y_o|^2 \qquad (6)$$

where F_o is the optimum noise figure, R_n the equivalent noise resistance, and $Y_o = G_o + jB_o$ the source admittance for optimum noise.

Typical results of the noise measurements are given in Figs. 10–15. The biaspoint dependence of the noise figure and associated gain for different sorts of MOSFET's is shown in Figs. 10–11. The additional noise figure $F-1$ is proportional to the inverse gain–bandwidth product C_{gs}/g_m, so the increase in F for $I_D \to 0$ is caused by the

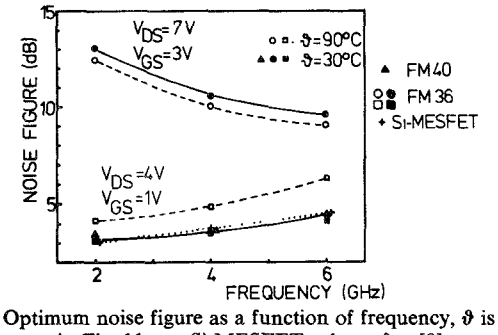

Fig. 12. Optimum noise figure as a function of frequency, ϑ is as given in Fig. 11. +: Si-MESFET values after [8].

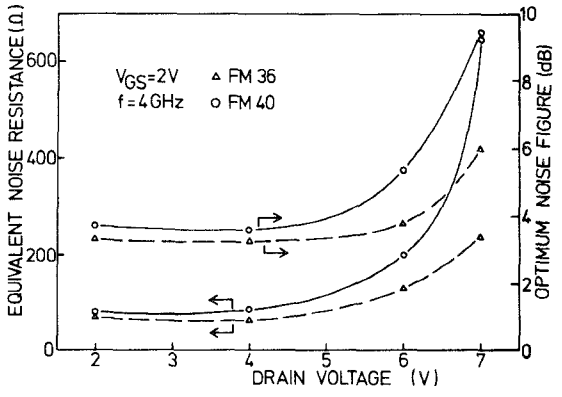

Fig. 13. Optimum noise figure F_o and equivalent noise resistance R_n of double implanted (○: FM 40) and unimplanted (Δ: FM 36) MOSFET's. The steep increase indicates avalanche noise.

decrease of g_m. Unimplanted devices are slightly less noisy than implanted ones, whereas the implanted devices show lower noise figure and gain variation over I_D. The latter MOSFET's would be more advantageous for circuit applications since they have a larger useful bias region. The noise figure and drain current dependence on drain-to-source voltage is given in Fig. 11. While trying to determine the origin for the steep increase in noise and drain current for $V_{DS} > 5.5$ V, we measured the noise figure at two different temperatures. In the ohmic and saturation region ($V_{DS} \leq 5$ V) the noise figure increases by increasing the chip temperature ϑ.

At higher voltages a different mechanism is responsible for the increased noise power produced by the MOSFET's. This process has a negative temperature coefficient. Such noise behavior is known from avalanche noise sources. The avalanche electric field of $3 \cdot 10^5$ V·cm^{-1} can be reached in the saturated part of the conducting inversion channel.

The interpretation of the excess current flow as a diffusion mechanism [7] would also predict an increase in diffusion noise power, but the temperature dependence of this mechanism has not yet been clarified. The avalanche at $V_{DS} > 6$ V also limits the signal power available from the MOSFET's, but since the avalanche multiplication is a self-stabilizing process, the devices withstand higher V_{DS} values of up to 12 V and V_{GS} values of up to 7 V without lasting changes in dc and RF characteristics.

The optimum noise figure is given in Fig. 12 as a function of frequency for two MOSFET types and also in

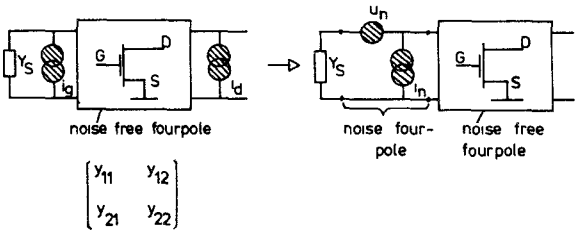

Fig. 14. Equivalent noise fourpole of Si-MOSFET's.

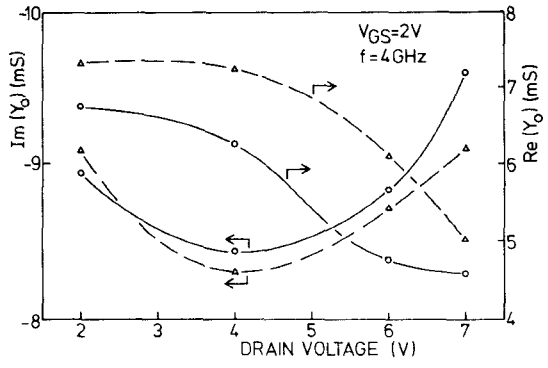

Fig. 15. Real and imaginary part of the optimum noise admittance Y_o of double implanted (○: FM 40) and unimplanted (Δ: FM 36) MOSFET's.

comparison with the noise figure of a 0.5-μm gate Si-MESFET after Bächtold *et al.* [8]. The Si-MOSFET values are quite equal to the Si-MESFET values, though the Si-MESFET had an f_{max} of 20 GHz instead of 10 GHz of our 0.8-μm Si-MOSFET's. The noise figure curves at $\vartheta = 90°C$ in Fig. 12 confirm the assumption of avalanche noise, being a broad-band phenomenon. The avalanche frequency should be less than 2 GHz as the curves for $V_{DS} = 7$ V show.

The detailed experimental noise analysis at 4 GHz showed all 4 noise parameters to increase slightly in magnitude with gate bias, at least for $V_{GS} > 2$ V. The drain voltage dependence of the noise parameters is given in Figs. 13 and 15.

The equivalent noise resistance R_n can reach values of over 600 Ω for implanted devices, whereas for unimplanted ones R_n reaches 240 Ω.

The increase of R_n that can be expressed by

$$R_n = \frac{\langle u_n^2 \rangle}{4kT_o \Delta f} \tag{7}$$

where u_n is the rms value of the noise voltage source of the noise fourpole after [9] (see also Fig. 14) is related to the increase of the noise current source i_d in shunt to the output of the MOSFET-fourpole (drain-to-source path):

$$\langle u_n^2 \rangle = \frac{|y_{11} + Y_s|^2}{|y_{21}|^2 \cdot |Y_s|^2} \cdot \langle i_d^2 \rangle. \tag{8}$$

Equation (8) means that increasing the channel noise source i_d will cause an increase of F_o and R_n in (6).

The same behavior can be stated for the optimum noise figure, where the implanted device FM 40 shows again the largest increase with drain voltage. Assuming that the excess noise is primarily effected by avalanche processes

and not by a hot electron effect, the conclusion is that implanted devices are more prone to avalanche than unimplanted ones. This can easily be understood since in implanted devices the acceptor concentration in the channel region is highly increased.

The real and imaginary parts of the optimum noise admittance are given in Fig. 15. The variation with V_{DS} is not large, especially for $B_o = \mathrm{Im}(Y_o)$. $G_o = \mathrm{Re}(Y_o)$ is more sensitive on V_{DS} variations and both implanted and not implanted devices have the same principal dependence. Comparing an average value of Y_o for the unimplanted MOSFET FM 36 of

$$Y_o = 6.2\ \mathrm{mS} - j \cdot 8.5\ \mathrm{mS} \tag{9}$$

with the corresponding S_{11}^* value of $20\ \mathrm{mS} \cdot (0.35 - j \cdot 0.6)$ shows a confined validity of the relation

$$y_o = \frac{Y_o}{20\ \mathrm{mS}} \approx S_{11}^*. \tag{10}$$

B. Large Signal Behavior

The large signal behavior of the fabricated MOSFET's was tested by measuring the output power as a function of the input power at 3 GHz to define the −1-dB compression point and by comparing the output harmonic distortion to GaAs MESFET-structures. Since all the tested MOSFET's have a gatewidth of 200 μm, the output power measurement is not very informative for high power structures. As has been mentioned in [10] the −1-dB output power was 30 mW at 3 GHz and a small signal gain of 4 dB. The power added efficiency amounted to 10 percent and the saturation power was 100 mW.

The harmonic distortion analysis of the Si-MOSFET's in comparison to buried channel GaAs MESFET's was carried out by feeding a 1-GHz signal from a 50-Ω generator with a harmonic purity of more than 65 dB to the test devices and measuring the output spectrum with an AILTECH 727 spectrum analyzer in the frequency range of 1 to 4 GHz. The spectral purity of the 1-GHz signal could be achieved by additional suppression of the harmonics via tuned variable shorts. The results are given on Figs. 16(a) and (b) together with typical dc characteristics of the tested devices.

The buried channel GaAs FET is superior in first-order harmonic distortion, (f=2 GHz) by nearly 5 dB in average up to an input power of 30 mW (Fig. 16(a)). At higher powers both devices showed similar behavior. The Si-MOSFET, on the other hand, has better second-order harmonic distortion (f=3 GHz) as can be seen by Fig. 16(b), also at input signal powers up to 50 mW. In Figs. 16(a) and (b) also the operating point of the two test devices is given in the dc characteristics.

The fact that the MOSFET's have a capacitive and not Schottky-diode gate as the GaAs MESFET's causes the latter ones to show higher dependence of the drain current on input power as can be seen on Table I. Here GaAs MESFET's of the recessed gate and the buried channel type are compared with double implanted Si-MOSFET's.

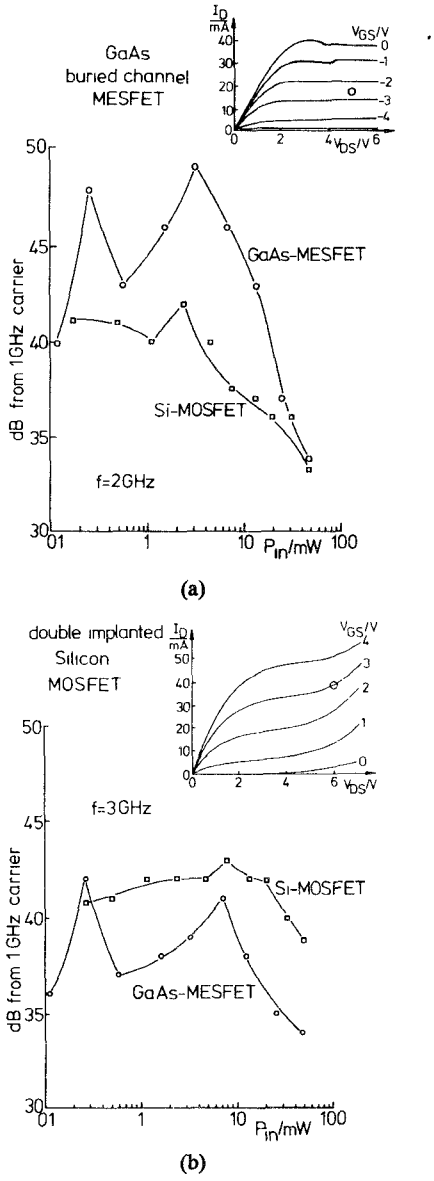

Fig. 16. Harmonic distortion of double implanted Si-MOSFET's (FM 38) in comparison to buried channel GaAs MESFET. Bias points are as given in the diagrams. (a) MOSFET: V_{DS}=6 V, V_{GS}=3 V. (b) MESFET: V_{DS}=5 V, V_{GS}=−2.5 V.

TABLE I
DEPENDENCE OF DRAIN CURRENT ON INPUT POWER FOR DIFFERENT FET TYPES

f=4 GHz	V_{DS}	V_{GS}	I_D (P_{in}=0.2 mW)	I_D (P_{in}=100 mW)
Si-MOSFET	4 V	3 V	35 mA	34 mA
Buried channel GaAs FET	4 V	−2 V	26 mA	17 mA
Recessed gate GaAsFET	4 V	−1 V	30 mA	34 mA

As given in [1] also the small and large signal switching behavior of the Si-MOSFET's has been tested in a 50-Ω measuring system. We measured an output pulse rise time of 48 ps and a delay time of 46 ps at a voltage gain of 1. Conclusions about the applicability of these devices in subnanosecond IC's will be possible when test circuits with 20-μm wide MOSFET's for lower power consumption will be fabricated.

V. Conclusion

Short channel silicon MOSFET's have been shown to be useful in the 2- to 6-GHz frequency band. The noise behavior is slightly better than that of a 1-μm Si-MESFET and equal to a 0.5-μm Si-MESFET up to 6 GHz. The optimum noise figure is 3–3.5 dB at 3.5 GHz. The maximum frequency of oscillation is of the order of 10 GHz, and model calculations showed f_{max} values of 13 GHz to be achievable by avoiding gate overlap. The Si-MOSFET's are more linear than recessed gate and buried channel GaAs MESFET's. Ion implantation, used to realize normally OFF-MOSFET's, only slightly affects the RF small signal gain and noise figure of the devices.

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References

[1] U. Niggebrügge *et al.*, "Implanted Si-MOSFETs for high speed applications," *Electron Lett.*, vol. 14, no. 21, p. 690, 1978.
[2] C. Tsironis and R. Stahlmann, "High frequency performance and equivalent circuit of implanted n-channel Si-MOSFET's," 5th Europ. Spec. Workshop Active Semicond. Dev. (Venice, Italy 1978).
[3] H. Beneking and H. Kasugai, "Gigahertz p-channel enhancement Silicon MOSFET with nonoverlapping Gate," *IEEE J. Solid-State Circuits*, vol. SC-5, p. 328, 1970.
[4] W. Bächtold and P. Wolf, "An improved microwave silicon MESFET," *Solid-State Electron.*, vol. 14, p. 783, 1971.
[5] T. Mimura *et al.*, "GaAs Microwave MOSFET's" *IEEE Trans. Electron. Dev.*, vol. ED-25, p. 573, 1978.
[6] C. Tsironis, "Einfluss der Technologie und der Parasitäten auf das Rauschverhalten von GaAs-MESFETs im GHz-Bereich," *Arch. Elek. Ubertragung*, vol. AEÜ-33, p. 32, 1979.
[7] E. Demoulin *et al.* "Bulk punchthrough characterization of Submicron Transistors using Poisson's equation," in *Proc. ESSDERC 1979 München*, p. 131.
[8] W. Bächtold *et al.*, "Si and GaAs 0.5 μm-Gate Schottky-Barrier Field-Effect Transistors," *Electron, Lett.*, vol. 9, p. 232, 1973.
[9] H. Rothe and W. Dahlke, "Theorie rauschender Vierpole," *Arch. Elek. Ubertragung*, vol. AEÜ-9, p. 117, 1955.
[10] C. Tsironis and U. Niggebrügge, "High frequency performance of implanted Si-MOSFETs," *MTT-S Symp., Dig. Tech. in Paper* Orlando, FL, pp. 396–398 1979.

A 4-W 56-dB Gain Microstrip Amplifier at 15 GHz Utilizing GaAs FET's and IMPATT Diodes

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***Abstract*—Performance results and design considerations are presented for an all solid-state *Ku*-band power amplifier which is feasible for use in PM communication systems for airborne or spacecraft transmitter applications. Design emphasis is placed on high power, and high efficiency operation as well as on compact amplifier construction. A six-stage GaAs FET preamplifier and a driver and balanced power amplifier utilizing GaAs IMPATT diodes operating in the injection locked oscillator mode are discussed. For high power and efficiency Schottky-Read IMPATT's with low-high-low doping profiles are employed. For improved reliability the IMPATT's incorporate a TiW barrier metallization to retard degradation of the IMPATT's. Results of accelerated life testing of the IMPATT devices are also presented.**

I. Introduction

THE USE OF solid-state devices for efficient amplification of CW microwave signals to power levels of several watts in the *Ku*-band frequency range is now possible with GaAs IMPATT diodes and to a lesser extent with GaAs FET's. Solid-state amplifiers of this type have obvious application in a wide variety of telecommunication systems both military and commercial, but are especially important for airborne and space applications where high efficiency, high reliability, and small physical size is essential. The purpose of this paper is to present the performance results and corresponding design considerations for an all solid-state microwave amplifier utilizing GaAs FET's and GaAs IMPATT diodes which is feasible for such applications. Specifically, a 15-GHz 4-W 56-dB gain microstrip amplifier whose design is relevant to a spacecraft communications transmitter employing digital phase modulation is considered. For high power and high efficiency, GaAs Schottky–Read IMPATT's with low-high-low doping profiles operating in the injection-locked oscillator (ILO) mode are used in the power stages. The diodes incorporate a platinum Schottky barrier contact with a titanium/tungsten barrier layer for improved reliability. Since the modulation in the transmitter application

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